THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte YOSHINORI KUNO and MASAHIDE HIRAMA

Appeal No. 96-1518
Application No. 08/190,244[1]

HEARD: March 12, 1999

Before HAIRSTON, BARRETT, and GROSS, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 2, 4, 5 and 7 through 12.

[1] Application for patent filed January 31, 1994. According to appellants, the application is a continuation of Application 07/957,148, filed October 7, 1992, now abandoned.

The disclosed invention relates to a MOS transistor formed on a semiconductor substrate. The MOS transistor has a pair of channel stoppers that are electrically connected to a source diffusion region formed on the surface of the semiconductor substrate in order to drive the channel stoppers in synchronism with the gate electrode of the MOS transistor.

Claim 10 is illustrative of the claimed invention, and it reads as follows:

10. A MOS transistor formed on a semiconductor substrate, comprising:

a source diffusion region formed on the surface of said semiconductor substrate;

a drain diffusion region formed on the surface of said semiconductor substrate at a position spaced apart from said source diffusion region;

a channel formed in the surface of said semiconductor substrate at a position between said source diffusion region and said drain diffusion region;

a first insulating layer formed on said semiconductor substrate;

a pair of channel stoppers formed in said first insulating layer at an adequate interval therebetween to determine the width of said channel, said pair of channel stoppers being composed of polysilicon;

a second insulating layer formed on said pair of channel stoppers;

a gate electrode formed on said channel and insulated therefrom by said first and/or second insulating layer while being insulated from said pair of channel stoppers by said second insulating layer; and

said pair of channel stoppers being electrically connected to the said source diffusion region to drive said channel stoppers in synchronism with said gate electrode.

The references relied on by the examiner are:

Sauer	4,603,426	July 29, 1986
Yamada	4,931,850	June 5, 1990
Kimura et al. (Kimura)	4,998,161	Mar. 5, 1991

Claims 2, 4, 5 and 7 through 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sauer in view of Kimura and Yamada.

Reference is made to the brief and the answer for the respective positions of the appellants and the examiner.

OPINION

The obviousness rejection is reversed.

Appellants and the examiner agree that Sauer merely shows a conventional charge detector (Figure 1) with load and drive transistors Q2 and Q3 in a source follower (Brief, page 4; Answer, page 3).

According to the examiner (Answer, page 3), "Kimura teaches an electrostatic screening electrode 31 formed perpendicular to and surrounding the gate electrode in order to prevent channels that might occur due to stray charge in these regions." Although the electrostatic screening electrode 31 in Kimura may function as a channel stopper, we agree with the appellants that it is not a pair of channel stoppers connected to "a source diffusion region, so that they are driven in synchronism with a gate electrode" (Brief, page 4).

The examiner states (Answer, page 3) that "Yamada in column 18 lines 35 et. seq. teaches to connect channel stops to the source electrodes of their adjacent transistors." Appellants argue (Brief, page 4) that in Yamada "the voltage levels on the channel stoppers are fixed to the voltage levels of the power supply, namely, the VSS and VDD, respectively." We agree with appellants that Yamada discloses connection of channel stopper 1110 to V_{SS} and connection of channel stopper 1117 to V_{DD} (column 18, lines 35 through 40).

In summary, we agree with appellants (Brief, page 4) that "[n]either of these references suggest connecting channel

stoppers to a source diffusion region, so that they are driven in synchronism with a gate electrode."

The obviousness rejection of claims 2, 4, 5 and 7 through 12 is reversed.

DECISION

The decision of the examiner rejecting claims 2, 4, 5 and 7 through 12 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)

lp

Appeal No. 96-1518
Application No. 08/190,244

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Appeal No. 96-1518
Application No. 08/190,244

APJ HAIRSTON

APJ BARRETT

APJ GROSS

DECISION: REVERSED
Send Reference(s): Yes No
or Translation (s)
Panel Change: Yes No
Index Sheet-2901 Rejection(s): _____

Prepared: September 27, 1999

Draft Final

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OB/HD GAU

PALM / ACTS 2 / BOOK
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